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Multi-physic Analysis for GaN Transistor PCB Layout

Bainan Sun, Kasper L  thje J  rgensen, Zhe Zhang, Michael A.E. Andersen

Department of Electrical Engineering

Technical University of Denmark

2800 Kongens Lyngby, Denmark

Email: baisun@elektro.dtu.dk, kalj@elektro.dtu.dk, zz@elektro.dtu.dk, ma@elektro.dtu.dk

Abstract—PCB layout for Gallium Nitride (GaN) transistor power loops are critical for achieving a stable operation in power converters. Optimal design should minimize the parasitic inductance as well as provide a low thermal resistance for heat dissipation. A multi-physic evaluation of performance between different PCB designs are made and a novel layout is proposed in this paper. The parasitic inductance and heat distribution of each layout are compared. The parasitic inductance is obtained from the oscillation frequency of the transistor drain-source voltage ringing. The thermal comparison is done with a combination of measurements and calculations. To ensure identical operating conditions, the buck converter adopts a modular design idea, where the plug-in totem poles of different designs are placed on the same motherboard. An optimized strategy for GaN transistor layout is given.

Index Terms—Gallium Nitride; PCB layout; parasitic inductance; thermal analysis; multi-physic simulation.

I. INTRODUCTION

GaN transistor has been introduced as a promising solution for high power density converter design [1] [2]. High frequency switching largely shrinks the volume of the converter passive components. However, at the same time, GaN transistor application introduces challenges in PCB layout [3]. Parasitic inductance from the PCB tracks will add considerable ringing to the transistor gate-source and drain-source voltage during the switching transients. Compared with Silicones and Silicone Carbide (SiC) transistor, GaN transistors are more vulnerable to voltage overshoot for the limited voltage rating and gate threshold. As a result, PCB layout for GaN transistor must be optimized to minimize the parasitic loop inductance [4].

The gate loop and the power loop of GaN transistor are the two critical loops considered for layout optimization [5]. For the optimal gate layout design, loop inductance must be minimized to avoid gate over voltage during turn-on transient and unintentional triggered-on during turn-off transient [6] [7]. The phenomenon of gate unintentional triggered can be further suppressed by applying negative gate voltage, while extra reverse conduction loss is introduced [8] [9]. Moreover, cross talk in GaN transistor totem pole should also be avoided by low capacitance design in gate loop layout and appropriate gate resistor selection [10] [11].

The power loop in a GaN transistor totem pole is composed of two transistors and the paralleled decoupling capacitors,

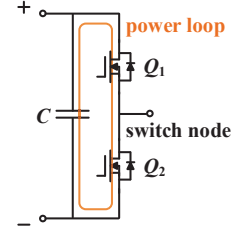


Fig. 1. Power loop in totem pole topology.

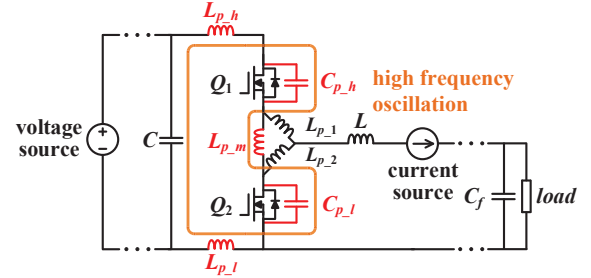


Fig. 2. Parasitic impedance in totem pole application.

which is shown in Fig. 1. The key issue of power loop layout optimization is to minimize the parasitic inductance. For a general voltage source converter application, the parasitic impedance in the totem pole is shown in Fig. 2. The switch node is viewed as a three-port impedance network in this paper. Parasitic inductance $L_{p,1}$ and $L_{p,2}$ are conducting respectively in the two steady-state conduction modes of totem pole transistors Q_1 and Q_2 . Influence of $L_{p,1}$ and $L_{p,2}$ is neglected under most circumstance when a relatively large inductor is series-connected as part of the output filter. Parasitic inductance $L_{p,h}$, $L_{p,m}$ and $L_{p,l}$, shown in Fig. 2, compose the power loop inductance, which is resonant with the transistor output capacitor $C_{p,h}$ and $C_{p,l}$ during the switching transient. The optimal power loop effectively reduces the power loop inductance and thus reduces the drain-source voltage ringing during hard switching operation [12] [13] [14]. Several power loop layout designs have been discussed in [15] [16]. Loop length minimization and magnetic canceling are applied to find the optimal layout. A multi-loop method for power loop layout is proposed in [17] and loop inductance is further

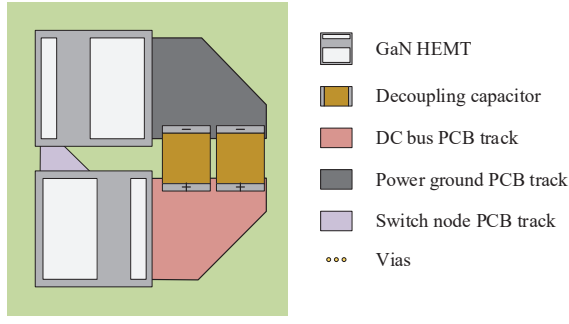


Fig. 3. Lateral layout.

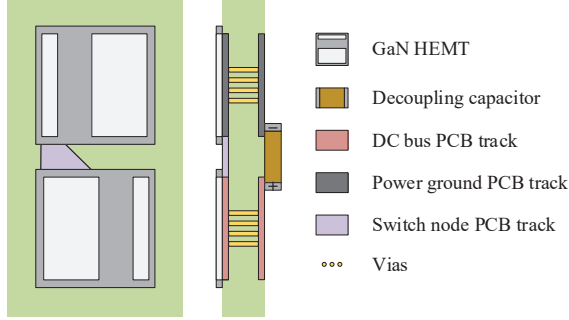


Fig. 4. Vertical layout.

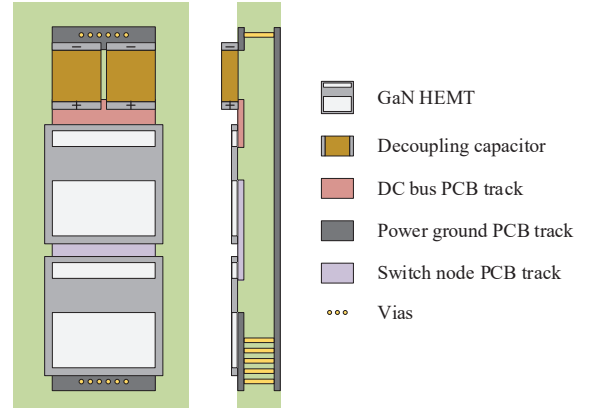


Fig. 5. Hybrid layout.

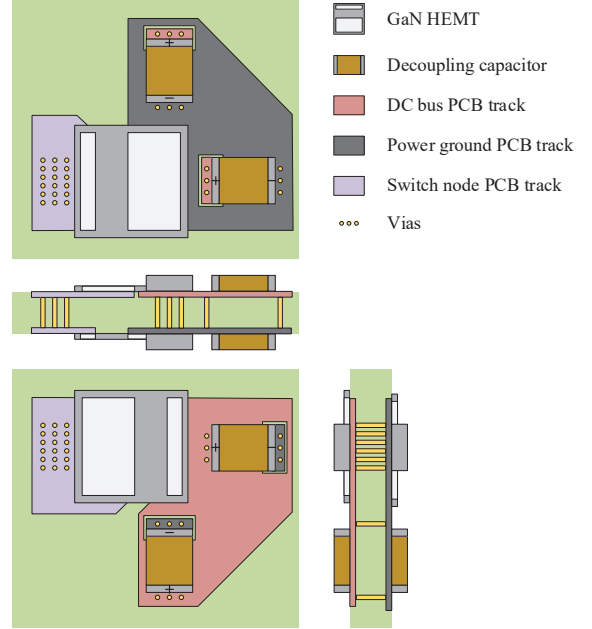


Fig. 6. Minimal layout.

reduced to 25% of the conventional design. Most of the earlier researches have focused on the land grid array (LGA) packaged GaN transistor. Voltage rating of the commercially available LGA packaged GaN transistors is limited to 350 V. Power loop layout optimization for 650 V rated GaNPX packaged transistors is rarely mentioned. Moreover, power dissipation and thermal design are critical in the application of high power rate GaN transistors. Evaluation of power loop layout considering both parasitic minimization and thermal dissipation is absent from the prior-art.

This paper provides a multi-physics evaluation of the different PCB layout designs in GaN transistor applications. Three conventional layout designs along with one novel minimal layout method are introduced in Section II. Section III elaborates the experimental measurement of power loop inductance. Comparison of the power loop inductance in each layout design is given. In Section IV, switching loss characterization is given with the double pulse test. Thermal analysis of different layout designs is carried out based on the loss decomposition and thermal image of modular buck converter operation. Conclusions are given in Section V.

II. POWER LOOP LAYOUT COMPARISON

A. Design Explanation

Evaluation of low inductance power loop layout is based on the application of 650 V, 15 A GaN transistor (GS66504B). The decoupling capacitors adopt the multi layer ceramic capacitor (MLCC), with a 500 V voltage rating and a 1812 package. Two layer FR4 PCB with the copper thickness of 2

oz is used. Creepage distance is chosen as 0.8 mm for each design, which applies for the generic PCB design standard (IPC-2221) at 500 V peak voltage isolation [18].

Lateral layout is shown in Fig. 3, which uses solely top layer for components placement and PCB layout. Distance between the decoupling capacitors and transistors is defined by the galvanic isolation clearance. Power loop length is minimized in the horizontal dimension. To further minimize the power loop, vertical layout is shown in Fig. 4. Vertical layout places the transistors in the top layer and decoupling capacitors in the bottom layer. Conduction between the two layers is completed by vias through the whole PCB board. Compared with lateral layout, power loop length is further reduced. Hybrid layout, shown in Fig. 5, adopts the idea of magnetic canceling to minimize the parasitic inductance. Transistors and decoupling capacitors are placed on the top layer, while the power return path is placed underneath. The power flow in these two layers

TABLE I
POWER LOOP LAYOUT COMPARISON

| | Dimensions | Lateral space | Vertical layer | Components placement |
|-----------------|-------------------|-----------------------|----------------|----------------------|
| lateral layout | 15.4 mm × 12.0 mm | 184.8 mm ² | 1 | one side |
| vertical layout | 12.7 mm × 12.0 mm | 152.4 mm ² | 2 | double side |
| hybrid layout | 7.9 mm × 21.8 mm | 172.2 mm ² | 2 | one side |
| minimal layout | 13.5 mm × 10.8 mm | 145.8 mm ² | 2 | double side |

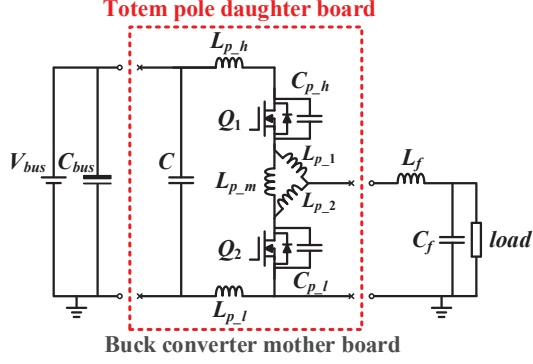


Fig. 7. Modular buck converter.

are in a reverse direction. Hence, the magnetic field excited by the current in these two layers are canceled and the parasitic inductance is reduced. A minimal layout is proposed in this paper, shown in Fig. 6. Two transistors are placed on the top and bottom layer respectively. Decoupling capacitors are also placed on both sides of the PCB, which helps to further reduce the power loop length. In the meantime, magnetic canceling is maintained by the opposite current flow direction in these two layers.

Power loop layout comparison is shown in TABLE I. Minimal layout takes the least lateral space and reduces 21 % lateral space taken compared with the lateral layout. Vertical layout also reduces 17.5 % of the space taken by the lateral layout. Both the minimal and vertical uses two sides of PCB to place component, which calls for challenge in manufacturing. Lateral space reduction in hybrid layout is not evident.

B. Modular Buck Converter

For comparing the different totem pole layouts, a buck converter is designed, as shown in Fig. 7. A modular design is adopted to guarantee identical test conditions for different layouts. The transistor totem bridge and decoupling capacitors, along with the gate driver and digital power supply, are placed on the daughter board. The rest of the buck converter, including DC bus capacitor and output filter, are placed on the mother board. Experimental setup is shown in Fig. 8. Digital controller DSP F28335 is used to apply gate signal via BNC coaxial cable. Lecroy passive probe (400 MHz band width, capacitance < 6 pF) is used to accurately measure the voltage signal. Ground connection of the probe uses the ground clip to reduce the extra parasitic inductance.

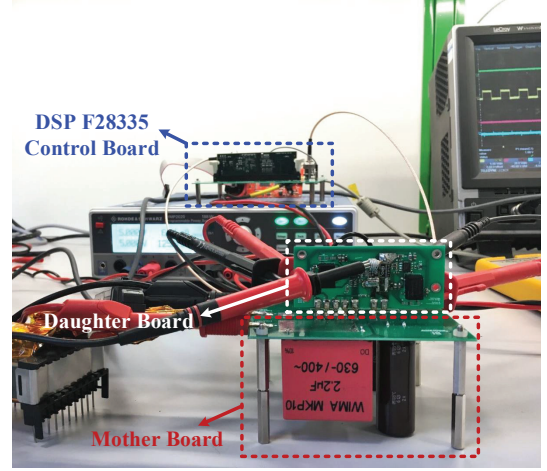


Fig. 8. Experimental setup.

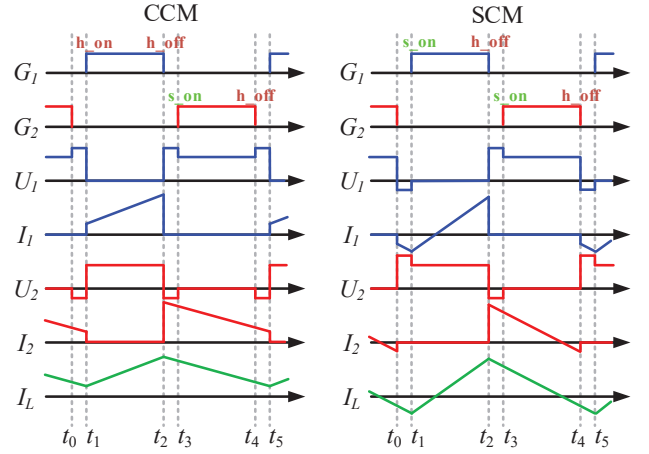


Fig. 9. Ideal waveform of the synchronous buck converter.

III. PARASITIC COMPARISON

A. Parasitic Analysis in Buck Converter

Synchronous buck converter has two operation modes: continuous conduction mode (CCM) and synchronous conduction mode (SCM), the ideal waveform of which is shown in Fig. 9. G_1 and G_2 are the gate signal of the high-side and low-side transistor. U_1 , U_2 and I_1 , I_2 are the drain-source voltage and source current of the high-side and low-side transistor respectively. I_L is the inductor current. Influence of the power

TABLE II
POWER LOOP INDUCTANCE COMPARISON

| | External capacitor | Total capacitance | Ringing frequency | Power loop inductance |
|-----------------|--------------------|-------------------|-------------------|-----------------------|
| lateral layout | 970 pF | 1301 pF | 74.9 MHz | 3.47 nH |
| vertical layout | 1020 pF | 1351 pF | 83.5 MHz | 2.69 nH |
| hybrid layout | 970 pF | 1301 pF | 86.2 MHz | 2.62 nH |
| minimal layout | 990 pF | 1321 pF | 90.8 MHz | 2.32 nH |

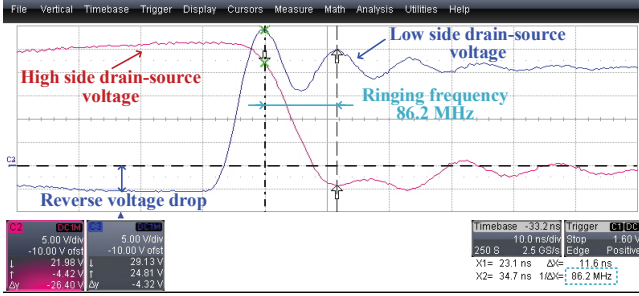


Fig. 10. Transistor drain-source voltage during the switching transient.

loop inductance is most evident in the hard switch on transient of the transistor. During this transient, the energy stored in the output capacitor of high side transistor is discharged within the power loop. Power loop inductance is resonant with the output capacitor of the low side transistor and lead to drain-source voltage ringing in the low side transistor, which must be minimized to avoid over voltage. Both the high side and the low side transistor is soft switched on in SCM. High side transistor is hard switched on in CCM.

The frequency of the voltage ringing can be calculated as

$$f_{sw} = \frac{1}{2\pi\sqrt{L_{total}C_{oss}}}, \quad (1)$$

where C_{oss} is the output capacitor of the low side transistor and L_{total} is total power loop inductance. It should be noted that L_{total} is the sum of all the inductive component along the power loop, including both PCB inductance and parasitic inductance within the device package. According to the measured ringing frequency, it is then possible to obtain this total loop inductance according to equation (1). However, the GaN transistor has a ultra low output capacitor (33 pF for the selected transistor at 400 V drain-source voltage). The frequency of the drain-source voltage ringing can be much higher than 500 MHz, which calls for difficulty in the practical measurement (limitation from the bandwidth of the probe and the oscilloscope).

B. Parasitic Inductance Comparison

To obtain the power loop inductance experimentally, an external capacitor is parallel connected to the low side transistor. The ringing frequency can be thus lowered and correctly measured. Furthermore, the parasitic inductance of the ground clip is decoupled by this external capacitance, which helps to

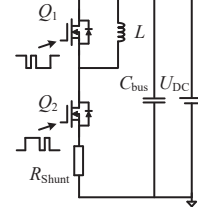


Fig. 11. Schematic of the double pulse test.

enhance the measurement accuracy. Selection of the external capacitance is a trade-off between the measurement accuracy and availability. Measurement accuracy is lowered with a low external capacitance and too large capacitance will damp out the voltage ringing. According to the analysis and experiment comparison, an optimal value of 1nF is selected as the external capacitor. Multi-layer ceramic capacitor (MLCC) in surface mount device (SMD) package is used for its ultra low parasitic inductance.

The measurement of power loop inductance is carried out in 20 V DC bus condition. External capacitor will largely slow down the switching transient and a low operating voltage will protect the half bridge from shoot through. Furthermore, the frequency of the voltage ringing is not relevant to the bus voltage, which guarantees the measurement accuracy. Experimental waveform is shown in Fig. 10. Buck converter operates in CCM and the high side transistor is in hard switching condition. The test results are summarized in TABLE II. Each external capacitor is individually measured before mounting on the PCB. The total parasitic capacitance within the power loop include the external capacitor, transistor output capacitor (325 pF at 20 V drain-source voltage) and the parasitic capacitance of the passive probe (6 pF). Lateral layout has the largest power loop inductance of 3.47 nH. Vertical and hybrid layout has similar power loop inductance and each reduces the power loop inductance by 24 %. The minimal layout has the lowest power loop inductance, which has a reduction of 33 % compared with the lateral layout.

IV. THERMAL ANALYSIS

A. Double Pulse Test

For the thermal analysis, the losses at different currents for the devices need to be known. A general method of determining the losses is by doing a double pulse test (DPT) [19]. The DPT circuit is shown in Fig. 11 and the experimental

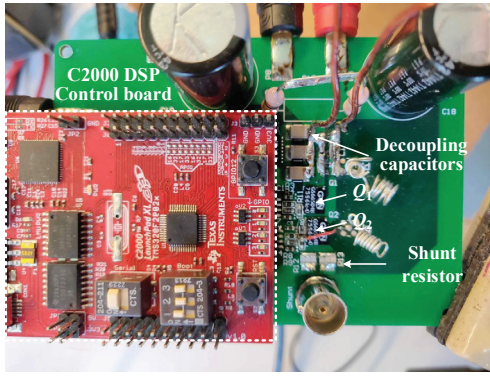


Fig. 12. Experimental setup of double pulse test.

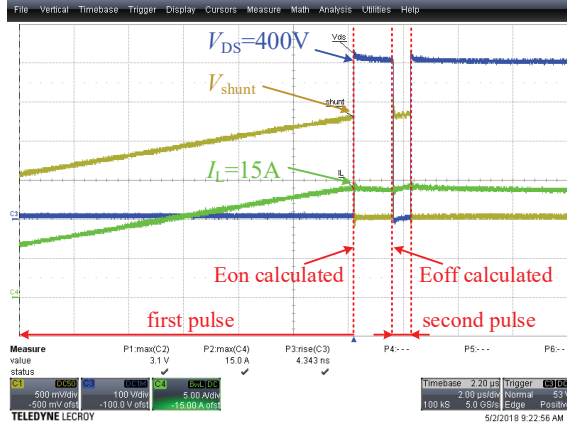


Fig. 13. Experimental waveform of the double pulse test.

setup is shown in Fig. 12. The double pulse tester used has a shunt resistor in the low side FET current path in order to measure the current, and adopts the hybrid layout strategy. It should be noted that the power loop inductance will not affect the switching loss calculation, which can thus be applied to a general loss estimation. Fig. 13 shows the current waveform and the drain-source voltage of the low side switch, and indicates the two switching moments used to measure the switching loss. The loss at different currents are shown in Fig. 14, and it is seen that switch-on has the higher loss than the switch-off transient.

B. Thermal Analysis

During the transistor operation, heat generated from the transistor junction is conducted to the PCB through the thermal pad of the transistor. Different layout methods varies in the thermal dissipation capability, which thus lead to difference in the operating temperature and the maximum switching power. The thermal evaluation of different layouts is first examined at a fixed switching condition. Four daughter boards based on the four layout methods are respectively plugged into the mother board to be switch at the same condition specified in TABLE III. Experimental waveform of the modular buck converter operation is shown in Fig. 15. The modular buck converter operates in SCM and both transistors in the half bridge are

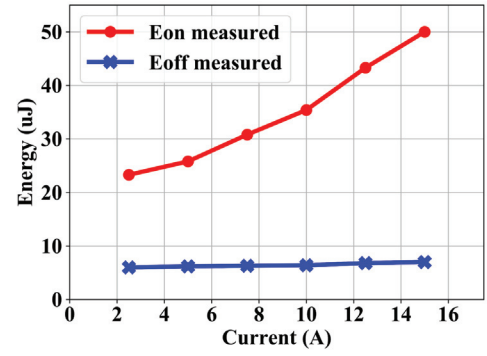


Fig. 14. Loss characterization from double pulse test.

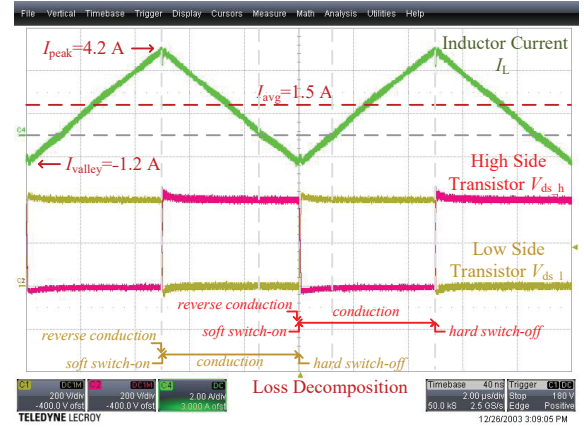


Fig. 15. Experimental waveform of the modular buck converter.

soft switched on. The total loss in each transistor includes conduction loss, reverse conduction loss and hard switched-off loss, which are calculated according to the data sheet from the manufacturer and the switching loss characterization from the double pulse test. It should be noted that the low side transistor has a higher power loss than the high side transistor, which is resulted from the difference in the reverse conduction current during the dead time. The thermal test is carried out at no air flow condition and no heat sink is installed. The room temperature is measured to be 24 °C.

The thermal distribution of each design during the fixed power test is shown in Fig. 16. Each result is captured when the thermal distribution and the transistor case temperature are stable after the consecutive operation of 5 minutes. The low side transistor always shows a higher temperature than the high side transistor, which is resulted from the extra reverse conduction loss. Minimal layout shows the lowest temperature, with a 10.5 °C temperature reduction in the low side transistor compared with the lateral layout. The junction-ambient thermal resistance of the minimal layout can thus be estimated to be 29.6 K/W. From the comparison of thermal image, it should be noted that the thermal distribution in the minimal layout is more uniform than the other three designs, which helps to reduce the thermal resistance.

TABLE III
SWITCHING CONDITION FOR THERMAL COMPARISON

| | | | |
|---------------------------|--------|--------------------------|-------|
| input voltage | 400V | output voltage | 200V |
| output power | 300W | output current | 1.5A |
| switching frequency | 100kHz | dead time | 100ns |
| on-state resistance | 100 mΩ | reverse voltage drop | 5V |
| high side transistor loss | 1.27W | low side transistor loss | 1.42W |

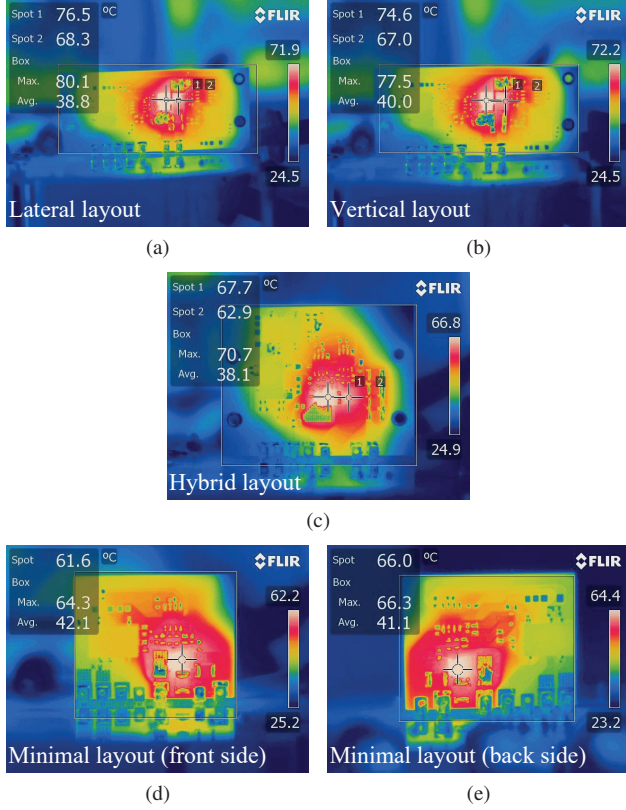


Fig. 16. Comparison of temperature distribution in each layout design.

TABLE IV
MAXIMUM POWER CAPABILITY

| Lateral layout | Vertical layout | Hybrid layout | Minimal layout |
|----------------|-----------------|---------------|----------------|
| 388 W | 400 W | 430 W | 440 W |

After the fixed power rate thermal test, each layout design is then tested to determine the maximum operation power. The operating condition maintains the same as the fixed power test and the output power is pushed to the limit restricted by the junction temperature. The normal operating junction temperature of the selected GaN transistor is specified as - 55 °C to +150 °C and the junction-case thermal resistance is specified to be 17 K/W from the transistor data sheet. Accordingly, the criteria for maximum power rate is defined when the transistor top-side case temperature 100 °C, which is a close approach to the junction thermal limit referred from

the thermal model. The result of maximum power test are summarized in TABLE IV. The minimal design shows the highest power rate, which can well handle the 440 W buck converter in SCM operation. The daughter board based on the hybrid layout shows a similar maximum power rate of 430 W. Lateral and vertical layout can handle 388 W and 400 W output power respectively.

V. CONCLUSIONS

This paper provides a multi-physic analysis of the power loop layout in GaN transistor application. Three conventional layout methods are elaborated. A novel minimal layout method is proposed in this paper, which can reduce the horizontal layout space by 21 % compared with the lateral layout. Power loop inductance in vertical layout is 23.4 % lower than the lateral layout, which validates the importance of conduction loop design and decoupling capacitor placement. Power loop inductance is further reduced in hybrid layout by the magnetic canceling. The minimal layout has the lowest power loop inductance of 2.32 nH, which is resulted from the short conduction loop. Minimal layout can also well handle the thermal dissipation, junction-to-ambient thermal resistance of which is calculated to be 29.6 K/W.

REFERENCES

- [1] A. Nawawi, C. F. Tong, S. Yin, A. Sakanova, Y. Liu, Y. Liu, M. Kai, K. Y. See, K. J. Tseng, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "Design and Demonstration of High Power Density Inverter for Aircraft Applications," *IEEE Transactions on Industry Applications*, vol. 53, no. 2, pp. 1168–1176, 2017.
- [2] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," *IEEE Energy Conversion Congress and Exposition: Energy Conversion Innovation for a Clean Energy Future, ECCE 2011, Proceedings*, pp. 2681–2688, 2011.
- [3] K. A. Kim, "Opening the Box: Survey of High Power Density Inverter Techniques From the Little Box Challenge," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 131–139, 2017. [Online]. Available: http://tpea.cpss.org.cn/uploads/soft/170801/1_1130473793.pdf
- [4] A. B. Jorgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jorgensen, and S. Munk-Nielsen, "A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices," *IEEE Transactions on Power Electronics*, vol. 1, no. c, 2018.
- [5] J. Wang and H. Shu-Hung Chung, "Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6672–6685, 2014.
- [6] A. Kulkarni, A. Gupta, and S. K. Mazumder, "Resolving Practical Design Issues in a Single-Phase Grid-Connected GaN-FET Based Differential-Mode Inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3734–3751, 2017.
- [7] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1484–1489, 2014.
- [8] P. M. Roschatt, S. Member, S. Pickering, and R. A. McMahon, "Bootstrap Voltage and Dead Time Behavior in GaN DC-DC Buck Converter With a Negative Gate Voltage," vol. 31, no. 10, pp. 7161–7170, 2016.
- [9] R. Hou, J. Xu, and D. Chen, "A multivariable turn-on/turn-off switching loss scaling approach for high-voltage GaN HEMTs in a hard-switching half-bridge configuration," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2017*, vol. 2017-Decem, pp. 171–176, 2017.

- [10] A. Gupta and S. K. Mazumder, "GaN-FET based grid-connected solar microinverter: Some design insights," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 233–237, 2017. [Online]. Available: <http://ieeexplore.ieee.org/document/8170552/>
- [11] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Cross conduction analysis for enhancement-mode 650-V GaN HFETs in a phase-leg topology," *WiPDA 2015 - 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications*, pp. 98–103, 2015.
- [12] H. Li, X. Li, Z. Zhang, C. Yao, and J. Wang, "Design consideration of high power GaN inverter," *WiPDA 2016 - 4th IEEE Workshop on Wide Bandgap Power Devices and Applications*, pp. 23–29, 2016.
- [13] J. Lautner and B. Piepenbreier, "Analysis of GaN HEMT switching behavior," *9th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2015-ECCE Asia*, pp. 567–574, 2015.
- [14] E. A. Jones, P. Williford, Z. Yang, J. Chen, F. Wang, S. Bala, J. Xu, and J. Puukko, "Maximizing the voltage and current capability of GaN FETs in a hard-switching converter," *Proceedings of the International Conference on Power Electronics and Drive Systems*, vol. 2017-Decem, no. December, pp. 740–747, 2018.
- [15] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high frequency gallium nitride based point of load converter," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, p. 1, 2013.
- [16] A. Letellier, M. Dubois, J. P. F. Trovao, and H. Maher, "Calculation of PCB Power Loop Stray Inductance in GaN or High di/dt Applications," *IEEE Transactions on Power Electronics*, vol. 8993, no. c, p. 1, 2018.
- [17] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DC-DC Converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4728–4740, 2017.
- [18] Institute of Printed Circuits (IPC), "IPC-2221A: Generic Standard on Printed Board Design," pp. 1–124, 2003. [Online]. Available: www.ipc.org
- [19] B. Sun, Z. Zhang, and M. A. Andersen, "Switching transient analysis and characterization of GaN HEMT," *IGBSG 2018 - 2018 International Conference on Intelligent Green Building and Smart Grid*, pp. 1–4, 2018.